

### Amendments to the Claims

This Listing of Claims will replace all prior versions, and listings, of claims in the instant application.

Please amend the claims as follows:

#### Listing of Claims:

1. (Currently amended) An integrated read-only memory, comprising:
  - selection transistors, each selection transistors having a drain connection;
  - an electrode for feeding a voltage or a current;
  - a common layer between the drain connections and the electrode electrically linking the drain connections to the electrode, wherein the electrical resistance of the common layer ~~can be changed through~~ is changeable by a configuration voltage or a configuration current;
  - a source connection per selection transistor; and
  - a bit line that is electrically connected to at least one source connection.
2. (Currently amended) The read-only memory of claim 1, wherein resistance of the common layer ~~can be~~ is configured to be switched over.
3. (Currently amended) The read-only memory of claim 1 or 2, wherein the resistance of the common layer ~~can be~~ is switched switchable ~~over~~ between two resistance characteristic curves.
4. (Currently amended) The read-only memory of claim 1 further comprising:
  - a read voltage applied to the common layer or a read current fed to the layer within a defined voltage or current range in a read Operation of the read-only memory, and
  - a configuration voltage or a configuration current outside the voltage or current range provided for the read Operation in a configuration operation of the read-only memory.

5. (Currently amended) The read-only memory of claim 1, wherein the read-only memory is ~~designed as~~ comprises a flash memory.
6. (Previously presented) The read-only memory of claim 1, wherein the selection transistors are arranged in an array.
7. (Previously presented) The read-only memory of claim 1, wherein the bit line is connected to a decoder circuit.
8. (Previously presented) The read-only memory of claim 1, wherein the bit line is accessible for an external connection.
9. (Previously presented) The read-only memory of claim 1, further comprising:
  - a gate connection per selection transistor, and
  - a word line that is electrically connected to at least one gate connection.
10. (Previously presented) The read-only memory of claim 9, wherein the word line is connected to a decoder circuit.
11. (Previously presented) The read-only memory of claim 9, wherein the word line is accessible for an external connection.
12. (Previously presented) The read-only memory of claim 1, wherein the selection transistors have a planar construction in the substrate.
13. (Previously presented) The read-only memory of claim 1, wherein the selection transistors have a vertical construction in the substrate.

14. (Currently amended) The read-only memory of claim 1, wherein the common layer is ~~formed as~~ comprises a molecular layer.

15. (Currently amended) The read-only memory of claim 14, wherein the common layer ~~contains~~ includes rotaxane.

16. (Currently amended) The read-only memory of claim 14, wherein the common layer ~~contains~~ includes catenane.

17. (Currently amended) The read-only memory of claim 14, wherein the common layer ~~contains~~ includes a bispyridinium compound.

18. (Currently amended) The read-only memory of claim 1, wherein the common layer is ~~formed as~~ comprises a dielectric.

19. (Currently amended) The read-only memory of claim 18, wherein the common layer ~~contains~~ includes  $\text{SrZrO}_3$ .

20. (Currently amended) The read-only memory of claim 1, wherein the common layer is ~~formed as~~ comprises a polymer.

21. (Currently amended) The read-only memory of claim 20, wherein the common layer ~~contains~~ includes 3-nitrobenzal malonitrile, 1,4-phenylenediamine complex.

22. (Currently amended) The read-only memory of claim 20, in which the common layer ~~contains~~ includes a chalcogenide compound.

23. (Currently amended) A method for operating an integrated read-only memory comprising selection transistors, each selection ~~transistors~~ transistor having a drain

connection; an electrode for feeding a voltage or a current; a common layer between the drain connections and the electrode electrically linking the drain connections to the electrode, the electrical resistance of the layer ~~can be changed through~~ is changeable by a configuration voltage or a configuration current; a source connection per selection transistor; and a bit line that is electrically connected to at least one source connection, the method comprising:

applying, in a read operation, a read voltage or a read current within a defined voltage or current range is applied to the common layer; and

applying, in a configuration operation, a configuration voltage or a configuration current outside the voltage or current range provided for the read operation to the common layer.

24. (Currently amended) A method for producing an integrated read-only memory, the method comprises:

producing selection transistors, each selection transistor having a drain contact;  
arranging an electrode;

providing a common layer between the drain connections and the electrode electrically linking the drain connections to the electrode, wherein the electrical resistance of the common layer ~~can be changed through~~ is changeable by a configuration voltage or a configuration current;

forming a source connection per selection transistor; and

forming a bit line which is electrically connected to at least one source connection.

25. (cancelled).

26. (Previously presented) The method for producing an integrated read-only memory of claim 24, wherein the selection transistors are produced in a front end process.

27. (Currently amended) The method for producing an integrated read-only memory of claim 24, wherein the common layer is deposited in a back end process.

28. (Previously presented) The method for producing an integrated read-only memory of claim 24, wherein the selection transistors are constructed in planar fashion in the substrate.
29. (Previously presented) The method for producing an integrated read-only memory of claim 24, wherein the selection transistors are constructed vertically in the substrate.
30. (Currently amended) The method for producing an integrated read-only memory of claim 24, wherein the providing a common layer is formed as comprises providing a molecular layer.
31. (Currently amended) The method for producing an integrated read-only memory of claim 30, wherein the common layer contains includes rotaxane.
32. (Currently amended) The method for producing an integrated read-only memory of claim 30, wherein the common layer contains includes catenane.
33. (Currently amended) The method for producing an integrated read-only memory of claim 30, wherein the common layer contains includes a bispyridinium compound.
34. (Currently amended) The method for producing an integrated read-only memory of claim 24, wherein the providing a common layer is formed as comprises providing a dielectric.
35. (Currently amended) The method for producing an integrated read-only memory of claim 34, wherein the common layer contains includes  $\text{SrZrO}_3$ .
36. (Currently amended) The method for producing an integrated read-only memory of 24, wherein the providing a common layer is formed as comprises providing a polymer.

37. (Currently amended) The method for producing an integrated read-only memory of claim 36, wherein the common layer ~~contains~~ includes a 3-nitrobenzal malonitrile, 1,4-phenylenediamine complex.

38. (Currently amended) The method for producing an integrated read-only memory of claim 29, wherein the common layer ~~contains~~ includes a chalcogenide compound.

39. (Previously presented) The method for producing an integrated of claim 24, wherein the selection transistors are produced using CMOS technology.